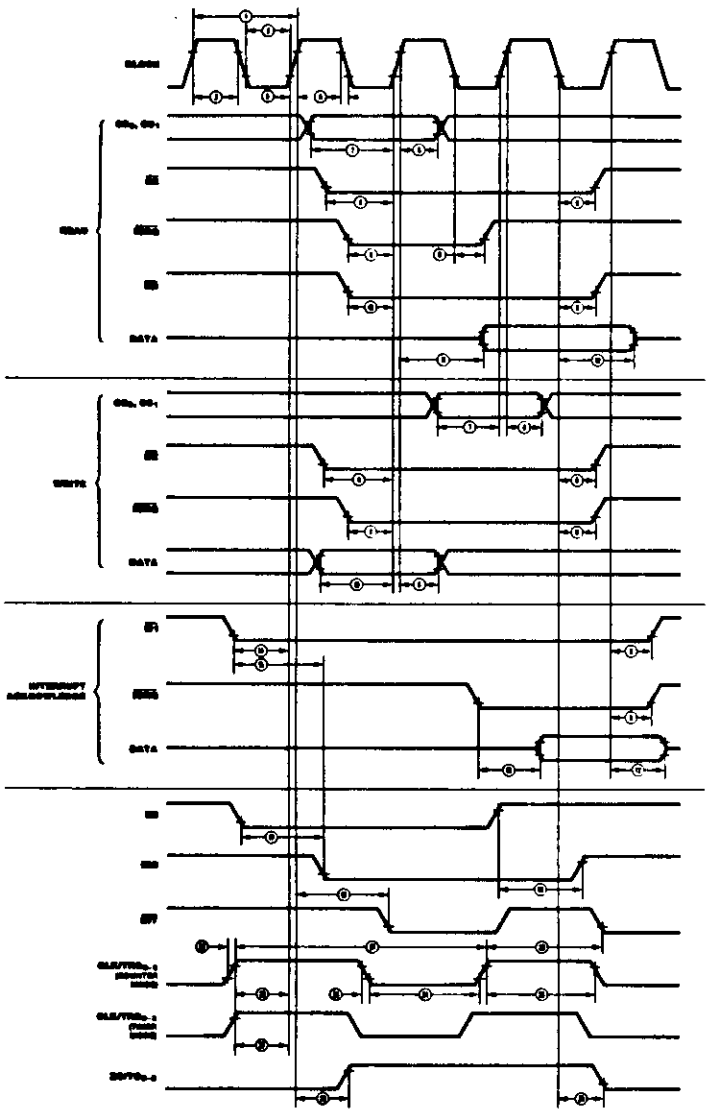
Distributed by:

JAMECO® ELECTRONICS

www.Jameco.com ✦ 1-800-831-4242

The content and copyrights of the attached material are the property of its owner.



Jameco Part Number 35609

Zilog

Z08430 Customer Procurement Spec (CPS)

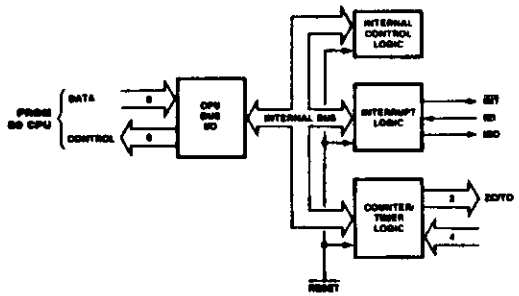
GENERAL DESCRIPTION

The Z80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes, a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in a 28-pin and a 44-pin chip carrier DIP.



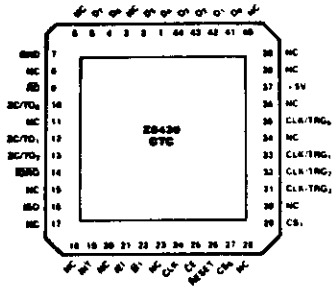
Functional Block Diagram

Z80 is a registered trademark of Zilog, Inc.

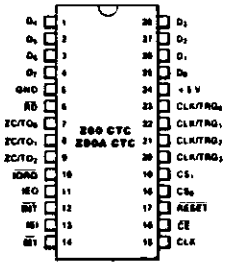
Copyright 1986 by Zilog, Inc.
All rights reserved. Specifications (parameters) on products delivered in the future are subject to change without notice. All parameters are tested, except those which are characterized or guaranteed by design.

Zilog, Inc. 1315 Dell Ave., Campbell, California 95008
Telephone (408)370-8000 TWX 910-338-7621

00-2840-01 Printed in USA



44-pin Chip Carrier, Pin Assignments



40-pin Dual-In-Line Package (DIP), Pin Assignments

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{ILC}	Clock Input Low Voltage	−0.3[c]	+0.45[a]	V	
V_{IHC}	Clock Input High Voltage	V_{CC} − 0.6[a]	V_{CC} + 0.3[c]	V	
V_{IL}	Input Low Voltage	−0.3[c]	+0.8[a]	V	
V_{IH}	Input High Voltage	+2.0[a]	V_{CC}[c]	V	
V_{OL}	Output Low Voltage		+0.4[a]	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4[a]		V	I_{OH} = −250 μA
I_{CC}	Power Supply Current		+120[a]	mA	
I_{LI}	Input Leakage Current		±10[a]	μA	V_{IN} = 0.4 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float		±10[a]	μA	V_{OUT} = 0.4 to V_{CC}
I_{OHD}	Darlington Drive Current	−1.5[a]		mA	V_{OH} = 1.5V R_{EXT} = 390Ω

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

AC CHARACTERISTICS

	Number	Symbol	Parameter	Z80 CTC Min	Z80 CTC Max	Z80A CTC Min	Z80A CTC Max	Z80B CTC Min	Z80B CTC Max	Notes†
a	1	TcC	Clock Cycle Time	400	[1]	250	[1]	165	[1]	
c	2	TwCh	Clock Width (High)	170	2000	105	2000	65	2000	
a	3	TwCl	Clock Width (Low)	170	2000	105	2000	65	2000	
a	4	TfC	Clock Fall Time		30		30		20	
a	5	TrC	Clock Rise Time		30		30		20	
c	6	Th	All Hold Times	0		0		0		
c	7	TsCS(C)	CS to Clock ↑ Setup Time	250		160		100		
a	8	TsCE(C)	$\overline{CE}$ to Clock ↑ Setup Time	200		150		100		
c	9	TsIO(C)	$\overline{IORQ}$ ↓ to Clock ↑ Setup Time	250		115		70		
a	10	TsRD(C)	$\overline{RD}$ ↓ to Clock ↑ Setup Time	240		115		70		
a	11	TdC(DO)	Clock ↑ to Data Out Delay		240		200		130	[2]
c	12	TdC(DOz)	Clock ↓ to Data Out Float Delay		230		110		90	
a	13	TsDI(C)	Data in to Clock ↑ Setup Time	80		50		40		
c	14	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		80		70		
a	15	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt immediately preceding M1)		300		190		130	[3]
a	16	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)		340		160		110	[2]
c	17	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		190		130		100	[3]
a	18	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (After ED Decode)		220		160		110	[3]
a	19	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		(1) + 200		(1) + 140		(1) + 120	[4,6]
a	20	TdCLK(INT)	CLK/TRG ↑ to $\overline{INT}$ ↓							
			tsCTR(C) satisfied		(19) + (26)		(19) + (26)		(19) + (26)	[5,6]
			tsCTR(C) not satisfied		(1) + (19) + (26)		(1) + (19) + (26)		(1) + (19) + (26)	[5,6]
a	21	TcCTR	CLK/TRG Cycle Time	2TcC		2TcC		2TcC		[5]
a	22	TrCTR	CLK/TRG Rise Time		50		50		40	
a	23	TfCTR	CLK/TRG Fall Time		50		50		40	
c	24	TwCTRl	CLK/TRG Width (Low)	200		200		120		
c	25	TwCTRh	CLK/TRG Width (High)	200		200		120		
a	26	TsCTR(Cs)	CLK/TRG ↑ to Clock ↑ Setup Time for Immediate Count	300		210		150		[5]
a	27	TsCTR(Ci)	CLK/TRG ↑ to Clock ↑ Setup Time for enabling of Prescaler on following clock ↑	210		210		150		[4]
a	28	TdC(ZC/TOr)	Clock ↑ to ZC/TO ↑ Delay		260		190		140	
a	29	TdC(ZC/TOf)	Clock ↓ to ZC/TO ↓ Delay		190		190		140	

NOTES:
[1] TcC = TwCh + TwCl + TrC + TfC
[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines and 100 pf for control lines
[3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum
[4] Timer mode
[5] Counter mode
[6] Parenthetical numbers reference the table number of a parameter e.g., (1) refers to TcC
† 2 ≤ TcC > (n − 2) TDM1(IEOf) + TDM1(IEOr) + TsIEI(IO) + TTL buffer delay if any. $\overline{RESET}$ must be active for a minimum of 3 clock cycles. Units are nanoseconds unless otherwise specified.

*Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
+ Timings are preliminary and subject to change. Units in nanoseconds.
a Tested
b Guaranteed by Design
c Guaranteed by Characterization